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ABSTRACT:
PROBLEM TO BE SOLVED: To reduce alpha rays emitted from a solder bump and reduce the soft error inversion ratio of a semiconductor device, by causing a solder alloy to be an alloy of Sn and Bi or an element having a specified atomic number and not related with specified alpha decay.

SOLUTION: A solder bump 12 is formed on a pad electrode of a semiconductor substrate 10 by a plating method and a solder ball, thus forming a semiconductor device 14. A solder alloy is caused to be an alloy of Sn and Bi or an element having an atomic number smaller than 81 and not related with alpha decay. Among elements having atomic numbers smaller than the atomic number 82 of Pb, there exists no element related with decay series, such as, U and Th. Therefore, no alpha decay is generated and hence no alpha ray is emitted. Thus, the soft error inversion ratio of the semiconductor device 14 may be reduced. Also, by reducing the quantity of alpha rays emitted from the solder alloy, the solder bump 12 may be arranged in a matrix. Therefore, finer pad diameter and pitch size of the bump are not necessary and deterioration in fatigue life of the solder bump 12 may be prevented.

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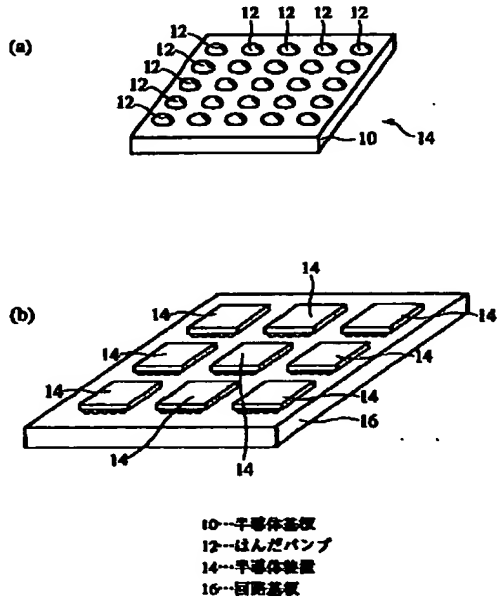
(54)【発明の名称】　半導体装置、回路基板及び電子回路装置

(57)【要約】

【課題】　フリップチップ接合法により半導体装置を回路基板等に接合する技術に関し、ソフトエラーを低減できる半導体装置、回路基板及び電子回路装置を提供する。

【解決手段】　半導体素子が形成された半導体基板と、半導体基板上に絶縁膜を介して形成され、半導体素子に接続された電極と、電極上に形成されたはんだ合金よりなるはんだバンプとを有する半導体装置において、はんだ合金を、Ｓｎと、Ｂｉ又は原子番号が８１未満のα崩壊に関与しない元素との合金により構成する。

本発明の第1実施形態による半導体装置の構造を示す概略図



10…半導体基板
12…はんだバンプ
14…半導体装置
16…回路基板

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【特許請求の範囲】

【請求項１】　半導体素子が形成された半導体基板と、前記半導体基板上に絶縁膜を介して形成され、前記半導体素子に接続された電極と、

前記電極上に形成されたはんだ合金よりなるはんだバンプとを有する半導体装置において、

前記はんだ合金は、Ｓｎと、Ｂｉ又は原子番号が８１未満のα崩壊に関与しない元素との合金であることを特徴とする半導体装置。

【請求項２】　請求項１記載の半導体装置において、

前記はんだ合金を構成するＳｎ中に含まれるＰｂの量が１ｐｐｍ以下であることを特徴とする半導体装置。

【請求項３】　請求項１又は２記載の半導体装置において、

前記はんだ合金は、前記Ｓｎを最多成分として含有することを特徴とする半導体装置。

【請求項４】　請求項１乃至３のいずれかに記載の半導体装置において、

前記半導体基板が前記はんだバンプによってフリップチップ接合された支持基板と、

前記半導体基板を覆うパッケージとを更に有することを特徴とする半導体装置。

【請求項５】　請求項４記載の半導体装置において、

前記半導体基板と前記支持基板の接合部における前記はんだ合金の形状は、中央部がくびれたウェスト形状であることを特徴とする半導体装置。

【請求項６】　支持基板と、

前記支持基板上に形成された電極と、

前記電極上に形成された請求項１乃至３のいずれかに記載のはんだバンプとを有することを特徴とする回路基板。

【請求項７】　回路基板と、

前記回路基板の表面にフリップチップ接合された請求項１乃至３のいずれかに記載の半導体装置とを有することを特徴とする電子回路装置。

【請求項８】　請求項７記載の電子回路装置において、

前記半導体装置と前記回路基板の接合部における前記はんだ合金の形状は、中央部がくびれたウェスト形状であることを特徴とする電子回路装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、フリップチップ接合法により半導体装置を回路基板等に接合する技術に係り、特に、フリップチップ接合法に適した半導体装置、回路基板及び電子回路装置に関する。

【０００２】

【従来の技術】従来より、ＬＳＩの端子パッドは、素子を配置した領域の外周部に形成されていた。素子と端子とを接合する代表的な接合方法としては、ワイヤボンディング法が主に用いられていた。しかし、近年のＬＳＩ

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の高集積化に伴い、入出力端子数の多端子化、端子間ピッチの微細化が進行し、従来の外周部へのパッド配置では対応しきれない場合が増加している。

【０００３】そこで、このような多端子化に対応するため、素子領域上にアレイ状にパッドを配置し、これをはんだバンプによって回路基板に実装するフリップチップ接合技術が開発されている。フリップチップ実装では、はんだバンプを用いて直接ＬＳＩと基板とを接合することから、信号を高速に伝搬できるという特徴がある。また、はんだバンプは、蒸着法或いはめっき法により形成できることから、端子の微細化に容易に対応できる等の特徴がある。

【０００４】なお、フリップチップ接合に用いるはんだ材料としては、Ｐｂ（鉛）を主成分としたＰｂ－Ｓｎ系の合金が主に用いられていた。

【０００５】

【発明が解決しようとする課題】はんだ材料として用いるＰｂには、２１４Ｐｂ、２１２Ｐｂ、２１０Ｐｂ、２０８Ｐｂ、２０６Ｐｂの５種類の同位体が含まれている。これら同位体は、Ｕ（ウラン）、Ｔｈ（トリウム）崩壊系列中の中間生成物、或いは最終生成物であり、崩壊の際にＨｅ原子核を放出するα崩壊を伴うことから、はんだ中よりα線が生じることがあった。

【０００６】このため、はんだバンプをＬＳＩの活性領域にアレイ状に配置するフリップチップ実装では、はんだバンプに含まれるＰｂの同位体及びα崩壊性不純物から発生するα線によってソフトエラーが生ずることがあった。一方、現在実用化されている最も高集積なＣＭＯＳデバイスでは、トランジスタのゲート長が０．５～０．７５μｍ、ソース－ドレイン間の電源電圧が２．５～３．０Ｖ程度であるが、これらの素子においては、古い鉱山から産出した、α崩壊に関与するＵ、Ｔｈ等の不純物含有量が少ないＰｂ（α線量が約１ｃｐｈ／ｃｍ^{2}程度）を用いてはんだを構成することによりソフトエラーを低減している。

【０００７】しかしながら、近年のＬＳＩの高集積化に伴いゲート数及び端子数は増加しており、素子から生じる発熱量を抑えるために電源電圧を低く設定する必要がある。これに伴い、N^+やP^+の拡散層中の最大収集電荷量も低くなる。また、集積度を上げるためにトランジスタのゲート長も微細化が進行している。このため、今後は電源電圧を２．０Ｖ以下に、ゲート長を０．２５μｍ以下に設定することが必須となるが、こうすることにより半導体素子はα線によって発生する擾乱電流に対してセンシティブになるため、ソフトエラーがおこりやすくなる虞がある。

【０００８】電源電圧が０．５Ｖ低くなると反転発生率は約２桁高くなり、ゲート長が減少すると収集電荷量も同様に減少することから、素子の微細化に伴いソフトエラー対策を強める必要があり、ソフトエラー率を低減で

きるはんだ材料が望まれていた。本発明の目的は、ソフトエラーを低減できるはんだ材料を提供し、更に、これをはんだバンプに用いた半導体装置、回路基板及び電子回路装置を提供することにある。

【０００９】

【課題を解決するための手段】上記目的は、半導体素子が形成された半導体基板と、前記半導体基板上に絶縁膜を介して形成され、前記半導体素子に接続された電極と、前記電極上に形成されたはんだ合金よりなるはんだバンプとを有する半導体装置において、前記はんだ合金は、Ｓｎと、Ｂｉ又は原子番号が８１未満のα崩壊に関与しない元素との合金であることを特徴とする半導体装置によって達成される。このように半導体装置を構成することにより、はんだバンプから発生するα線を減少することができる。これにより、半導体装置のソフトエラー反転率を大幅に低減することができる。

【００１０】また、はんだ合金から発生するα線量を低減することにより、はんだバンプをマトリクス状に配置することができるので、バンプのパッド径、ピッチサイズを微細化する必要もなく、はんだバンプの疲労寿命の低下を防止することができる。また、半導体装置の微細化・電源電圧の低電圧化が更に進んだ場合にも、ソフトエラーを効果的に防止することができる。

【００１１】また、上記の半導体装置において、前記はんだ合金を構成するＳｎ中に含まれるＰｂの量が１ｐｐｍ以下であることが望ましい。このようにＰｂの含有量を減少することにより、α崩壊する確率を従来の１／１０～１／１００以下に低減することができる。従って、ソフトエラー率を大幅に低減することができる。また、上記の半導体装置において、前記はんだ合金は、前記Ｓｎを最多成分として含有することが望ましい。

【００１２】また、上記の半導体装置において、前記半導体基板が前記はんだバンプによってフリップチップ接合された支持基板と、前記半導体基板を覆うパッケージとを更に有することが望ましい。このように半導体装置を構成すれば、ソフトエラー耐性の強い半導体パッケージを形成することができる。また、上記の半導体装置において、前記半導体基板と前記支持基板の接合部における前記はんだ合金の形状は、中央部がくびれたウェスト形状であることが望ましい。このように半導体装置を構成すれば、電極にかかる応力を分散することができるので、はんだの疲労寿命の低下を防止することができる。

【００１３】また、支持基板と、前記支持基板上に形成された電極と、前記電極上に形成された上記のはんだバンプとを有することを特徴とする回路基板によっても達成される。このように回路基板を構成することにより、回路基板上に半導体装置を搭載した場合のソフトエラー発生を低減することができる。また、回路基板と、前記回路基板の表面にフリップチップ接合された上記の半導体装置とを有することを特徴とする電子回路装置によっても達成される。このように電子回路装置を構成すればソフトエラーによる半導体装置の誤動作等を減少できるので、電子回路装置の信頼性を高めることができる。

【００１４】また、上記の電子回路装置において、前記半導体装置と前記回路基板の接合部における前記はんだ合金の形状は、中央部がくびれたウェスト形状であることが望ましい。このように半導体装置を構成すれば、電極にかかる応力を分散することができるので、接合部の疲労寿命の低下を防止することができる。これにより、電子回路装置の信頼性を向上することができる。

【００１５】

【発明の実施の形態】本発明の第１実施形態による半導体装置について図１及び図２を用いて説明する。図１は本実施形態による半導体装置の構造を示す概略図、図２は本実施形態の変形例による半導体装置の構造を示す概略断面図である。

【００１６】従来より、α線によるソフトエラーを防止する方法としては、チップ表面にα線遮蔽効果のあるコーティング剤を塗布する方法、ＬＳＩ上のバンプのレイアウトを変えてα線源と素子までの距離を大きくする方法、誤り訂正などのシステム的な保護手段を設ける方法、はんだ材料に含まれるα線源となる不純物量を低減する方法、などが用いられていた。

【００１７】従来のＣＭＯＳデバイスでは、α線源と活性領域までの距離が極力離れるようバンプを配置し、ソフトエラー反転の防止を行ってきた。しかし、今後ますます集積度が高くなると素子上にもはんだバンプを配置する必要が生じる。また、バンプのレイアウト変更によるα線防止を行うと、バンプのパッド径、ピッチサイズを更に微細化する必要があるが、この場合においても繰り返しかかる応力による疲労寿命を十分確保する必要がある。

【００１８】これらの方法に対し、はんだ材料に含まれるα線源を低減する方法は非常に有効である。しかし、従来用いられていたＳｎ－Ｐｂ系はんだにおいては、α崩壊に関与するＰｂの同位体を除去することは通常の化学処理等では不可能であり、材料コストの面から好ましくなかった。

【００１９】そこで、本願発明者等は、ソフトエラーを低減する手段として、従来のＰｂの代わりにα崩壊に関与しない材料を用いてはんだを構成することを考えた。具体的には、Ｂｉ（ビスマス）、又は、Ｐｂより原子番号が小さい元素で構成される、Ｓｎ（錫）をベースにしたはんだを用いることに思い至った。すなわち、原子番号がＰｂの８１より小さい元素においては、Ｕ、Ｔｈなどの崩壊系列に関わる元素が存在しないため、α崩壊が発生しないためα線が生じることがないからである。また、Ｂｉについては、Ｕ、Ｔｈ等の崩壊系列に同位体が存在するものの、その半減期が１９．９分と短く、その同位体の存在比も少ないため、高純度化が容易だからで

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ある。

【００２０】この場合、各元素に不純物として崩壊系列にかかわる元素が含有されていても、Ｐｂの場合の同位体除去に比べて材料の高純度化は比較的容易であり、材料コストを安くすることができる。なお、原子番号がＰｂの８１より小さい元素としては、例えばＳｂ（アンチモン）、Ａｇ（銀）、Ｚｎ（亜鉛）などを用いることができる。

【００２１】更に、本願発明者は、はんだの構成元素については、Ｐｂ含有量をそれぞれ低減することが重要であることを見いだした。例えば、従来より用いられているＳｎ－Ｓｂ系はんだは少量のα線を放出するが、Ｓｎ－Ｓｂはんだ中からα崩壊に関与するＵやＴｈを可能な限り除去しても、α線量を十分に低減することはできなかった。

【００２２】この原因について本願発明者等が調査した結果、Ｓｎ中に不純物として含まれるＰｂの同位体（特に、半減期の短い２１４Ｐｂ、２１２Ｐｂ、２１０Ｐｂ）のα崩壊によりα線が発生していることを見いだした。そこで、Ｓｎ中の含有Ｐｂ量を減少したところ、α線量を低減できることが判った。すなわち、Ｐｂ濃度を１ｐｐｍ以下に抑えることにより、α崩壊する確率を従来の１／１０～１／１００以下に低減することができた。

【００２３】次に、上記のはんだをはんだバンプとして用いた半導体装置を構成し、ソフトエラー耐性について評価を行った結果について示す。まず、ｐ型のシリコン基板上に、通常のＭＯＳトランジスタの製造プロセスにより、ｎ型ＭＯＳトランジスタ及びｐ型ＭＯＳトランジスタにより構成されるＣＭＯＳデバイスを形成した。

【００２４】次いで、ＣＭＯＳデバイスを形成したシリコン基板上に、膜厚約５００ｎｍの絶縁層を介して、膜厚約１μｍのＡｌ（アルミ）よりなる配線層と、膜厚約

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１００ｎｍのＴｉ（チタン）膜と、膜厚約２００ｎｍのＮｉ（ニッケル）膜と、膜厚約２００ｎｍのＡｕ（金）膜よりなるパッド電極を形成した。こうして、半導体素子が形成され、その表面にマトリクス状にパッド電極が形成された半導体基板１０を形成した。

【００２５】続いて、表１に示す種々のはんだ合金を用い、半導体基板１０のパッド電極上にめっき法及びはんだボールによってはんだバンプ１２を形成し、半導体装置１４を形成した（図１（ａ））。なお、はんだ合金を構成するＳｎ原料には、Ｐｂの含有不純物濃度が１ｐｐｍ以下のものを用いた。この後、このように形成した半導体装置１４の表面にフラックスを塗布し、コンベア炉内でＡｌＮよりなる回路基板１６上にフリップチップ接合した（図１（ｂ））。このとき、はんだバンプ１２の径は１００μｍであり、はんだバンプ１２間のピッチは２１０μｍであった。

【００２６】このように回路基板１６上に搭載した半導体装置１４についてソフトエラー反転率を測定した。なお、ソフトエラー反転率は、Ｐｏ（ポロニウム）標準試料（放射線量：８．０×10^{-3}Ｂｑ）を用いてα線を半導体装置１４に対し発生させ、テスターにより測定した。また、はんだ材料中のα線量はα－トラック法によって測定した。

【００２７】その結果、表１に示すように、Ｐｂの代わりに、Ｂｉ又はＰｂより原子番号が小さい元素で構成される、Ｓｎをベースにしたはんだを用いることにより（実施例１乃至実施例１６）、ソフトエラー反転率は10^{-2}ｆｉｔ／ｂｉｔ以下の値を得ることができた。すなわち、比較例１、２に示した従来のＰｂ－５ｗｔ％Ｓｎはんだと比較して、２桁以上低いソフトエラー反転率を達成することができた。

【００２８】

【表１】

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	はんだ合金（組成はwt%）	α線量 cph/cm²	純度	Sn中のPb量 ppm	ソフトエラー反転率 fit/bit
実施例1	95Sn-5Zn	<0.1	5N	<1	<0.01
実施例2	90Sn-10Zn	<0.1	5N	<1	<0.01
実施例3	95.5Sn-3.5Ag-1Zn	<0.1	5N	<1	<0.01
実施例4	92Sn-3Ag-5Zn	<0.1	5N	<1	<0.01
実施例5	88Sn-2Ag-10Zn	<0.1	5N	<1	<0.01
実施例6	95Sn-5Sb	<0.1	5N	<1	<0.01
実施例7	90Sn-10Sb	<0.1	5N	<1	<0.01
実施例8	95.5Sn-3.5Ag-1Sb	<0.1	5N	<1	<0.01
実施例9	92Sn-3Ag-5Sb	<0.1	5N	<1	<0.01
実施例10	88Sn-2Ag-10Sb	<0.1	5N	<1	<0.01
実施例11	95Sn-5Bi	<0.1	5N	<1	<0.01
実施例12	90Sn-10Bi	<0.1	5N	<1	<0.01
実施例13	95.5Sn-3.5Ag-1Bi	<0.1	5N	<1	<0.01
実施例14	92Sn-3Ag-5Bi	<0.1	5N	<1	<0.01
実施例15	88Sn-2Ag-10Bi	<0.1	5N	<1	<0.01
実施例16	96.5Sn-3.5Ag	<0.1	5N	<1	<0.01
比較例1	5Sn-95Pb	1.0	4N		0.1
比較例2	5Sn-95Pb	10.0	4N		1

従って、このようなはんだ合金を用いてフリップチップ接合用のはんだバンプを形成すれば、半導体装置のソフトエラー反転率を大幅に低減することができる。また、はんだ合金から発生するα線量を低減することにより、はんだバンプをマトリクス状に配置することができるので、バンプのパッド径、ピッチサイズを微細化する必要もなく、はんだバンプの疲労寿命の低下を防止することができる。

【００２９】また、半導体装置の微細化・電源電圧の低電圧化が更に進んだ場合にも、ソフトエラーを効果的に防止することができる。なお、上記実施形態では、半導体装置を回路基板上に接合する場合について説明したが、半導体装置は他の基板に接合してもよい。例えば、図２に示すように、基板１８上に接合された半導体装置１４にキャップ２０をかぶせ、半導体パッケージ２２を形成してもよい。また、回路基板上に半導体装置を接合し、マルチチップモジュールを形成してもよい。

【００３０】また、上記実施形態において、はんだ合金を構成する際には、はんだ合金中の最多成分がＳｎとなるようにすることが効果的である。次に、本発明の第２実施形態による半導体装置について図３乃至図６を用いて説明する。図３はＳｎ－Ｓｂ系はんだの引っ張り強度とＳｂ添加量との関係を示すグラフ、図４ははんだバンプの形状による問題を説明する図、図５は本実施形態による半導体装置の構造を示す概略図、図６は本実施形態において疲労寿命試験を行った手順を示す図である。

＊【００３１】第１実施形態におけるＳｎ系はんだを用いてフリップチップ接合用のはんだバンプを形成すれば、半導体装置のソフトエラー反転率を大幅に低減することができる。しかしながら、上記のＳｎ系はんだは、その硬度がＳｎ－Ｐｂ系はんだと比較して硬い。例えば、Ｓｎ－Ｓｂ系はんだでは、図３に示すように、その引っ張り強度は７～１５ｋｇｆ／ｍｍ²であり、Ｓｎ－Ｐｂ系はんだの３．５ｋｇｆ／ｍｍ²よりも大きい。

【００３２】このため、例えば、図４に示すようなはんだバンプ１２を用いてはんだ接合を行うと、接合の際に電極２４、２６に応力が集中し、疲労寿命の低下をもたらすことが懸念される。本実施形態では、接合の際に電極に応力が集中しない半導体装置の構造について示す。

【００３３】本実施形態による半導体装置は、接合後のはんだ合金の形状が、その中央部がくびれたウェスト形状となるように構成していることに特徴がある。すなわち、半導体基板１０に形成された電極２４上には、その上部ほど細くなるように形成されたはんだバンプ１２が形成されている。一方、半導体装置１４を搭載する回路基板１６上の電極２６上にも、その上部ほど細くなるように形成されたはんだバンプ１２が形成されている。また、回路基板１６には更に、接合する半導体基板１０と回路基板１６との距離を所定の値にするためのスタッドバンプ２８が形成されている。

【００３４】このようにして形成された半導体装置１４を回路基板１６に接合すると、半導体装置１４のはんだ

バンプ１２と、回路基板１６のはんだバンプ１２とにより、その中央部がくびれたはんだ合金による接合３０が形成される。半導体装置１４と回路基板１６との間の間隔は、スタッドバンプ２８により所望の距離に制御されている。

【００３５】このようなはんだバンプ１２を有する半導体装置１４及び回路基板１６を構成することにより、接合の際に電極２４、２６に与える応力集中を軽減することができるので、上記のＳｎ系はんだを用いてフリップチップ接合を行った場合にも、はんだ接合部の疲労寿命の低下を抑制することができる。次に、本実施形態による半導体装置について疲労寿命評価を行った結果を図６を用いて説明する。

【００３６】まず、疲労寿命評価用のサンプルとして、電極２４をマトリクス状に配置した１３ｍｍ角の半導体基板１０を作成した。電極２４は、膜厚約１００ｎｍのＴｉ膜と、膜厚約２００ｎｍのＮｉ膜と、膜厚約２００ｎｍのＡｕ膜を、スパッタ法により順次堆積した積層膜により形成した。次いで、はんだ材料中のＰｂ濃度を１ｐｐｍ以下にしたＳｎ－５ｗｔ％Ｓｂ合金をはんだ合金として用い、回路基板１６の電極２６上及び半導体基板１０の電極２４上にはんだバンプ１２を形成した。また、回路基板１６上の四隅には、Ａｕよりなるスタッドバンプ２８を形成した。スタッドバンプの高さは、接合後のはんだバンプの高さが１２０μｍとなるように調整した。

【００３７】はんだバンプは、図６（ａ）に示すように、メタルマスク３２により半導体基板１０を覆った後、はんだ合金１２を蒸着することにより形成した。このようにしてはんだバンプ１２を形成することにより、その上部ほど細い形状のはんだバンプ１２を形成することができる（図６（ｂ））。このようにして、はんだバンプ１２が半導体基板１０上に形成された半導体装置を形成した。

【００３８】続いて、表面にフラックスを塗布した後、半導体装置１４と回路基板１６の位置合わせを行い（図６（ｃ））、コンベア炉中でリフローを行うことにより半導体装置１４と回路基板１６とのフリップチップ接合を行った（図６（ｄ））。このようにして接合した接合３０は、その径が約１００μｍ、バンプ間のピッチが２１０μｍ、バンプ高さが１２０μｍのウェスト形状であった。

【００３９】この後、このように形成したフリップチップ接合体を－６５～１２５℃の熱衝撃試験を行った結果、１００サイクルの試験をクリアすることができ、Ｐｂ－５ｗｔ％Ｓｎはんだと同程度の疲労寿命を有していることが判った。このように、本実施形態によれば、第１実施形態におけるＳｎ系はんだを用い、接合後のはんだバンプの形状が、その中央部がくびれたウェスト形状となるように構成したので、接合の際に電極に応力が集中することを抑制することができる。これにより、Ｐｂ－Ｓｎ系はんだと同等の疲労寿命を確保することができる。

【００４０】また、本実施形態では、回路基板１６上の電極２６にも第１実施形態による半導体装置に用いたはんだ合金を適用しているので、半導体装置が回路基板に搭載された電子回路装置の信頼性をも高めることができる。なお、上記実施形態では、半導体装置を回路基板に搭載する場合について説明したが、図２に示す半導体パッケージを形成する際にも適用することができる。すなわち、半導体装置１４を基板１８に接合する際に、図６に示す方法により行うことができる。

【００４１】

【発明の効果】以上の通り、本発明によれば、上記目的は、半導体素子が形成された半導体基板と、半導体基板上に絶縁膜を介して形成され、半導体素子に接続された電極と、電極上に形成されたはんだ合金よりなるはんだバンプとを有する半導体装置において、はんだ合金として、Ｓｎと、Ｂｉ又は原子番号が８１未満のα崩壊しない元素との合金を用いるので、はんだバンプから発生するα線を低減することができる。これにより、半導体装置のソフトエラー反転率を大幅に低減することができる。

【００４２】また、はんだ合金から発生するα線量を低減することにより、はんだバンプをマトリクス状に配置することができるので、バンプのパッド径、ピッチサイズを微細化する必要もなく、はんだバンプの疲労寿命の低下を防止することができる。また、半導体装置の微細化・電源電圧の低電圧化が更に進んだ場合にも、ソフトエラーを効果的に防止することができる。

【００４３】また、上記の半導体装置において、はんだ合金を構成するＳｎ中に含まれるＰｂの量を１ｐｐｍ以下にすれば、α崩壊する確率を従来の１／１０～１／１００以下に低減することができる。これにより、ソフトエラー率を低減することができる。また、上記の半導体装置において、はんだ合金はＳｎを最多成分として含有することが望ましい。

【００４４】また、上記の半導体装置において、半導体基板がはんだバンプによってフリップチップ接合された支持基板と、半導体基板を覆うパッケージとを更に設ければ、ソフトエラー耐性の強い半導体パッケージを形成することができる。また、上記の半導体装置において、半導体基板と支持基板の接合部におけるはんだ合金の形状を、中央部がくびれたウェスト形状にすれば、電極にかかる応力を分散することができるので、はんだの疲労寿命の低下を防止することができる。

【００４５】また、支持基板と、支持基板上に形成された電極と、電極上に形成された上記のはんだバンプとにより回路基板を構成するので、この回路基板上に半導体装置を搭載した場合のソフトエラー発生を低減すること

ができる。また、回路基板と、回路基板の表面にフリップチップ接合された上記の半導体装置とにより電子回路装置を構成すれば、ソフトエラーによる半導体装置の誤動作等を減少できるので、電子回路装置の信頼性を高めることができる。

【００４６】また、上記の電子回路装置において、半導体装置と回路基板の接合部におけるはんだ合金の形状を、中央部がくびれたウェスト形状にすれば、電極にかかる応力を分散することができるので、はんだの疲労寿命の低下を防止することができる。

【図面の簡単な説明】

【図１】本発明の第１実施形態による半導体装置の構造を示す概略図である。

【図２】本発明の第１実施形態の変形例による半導体装置の構造を示す概略断面図である。

【図３】Ｓｎ－Ｓｂ系はんだの引っ張り強度とＳｂ添加量との関係を示すグラフである。

【図４】はんだバンプの形状による問題を説明する図である。

【図５】本発明の第２実施形態による半導体装置の構造を示す概略図である。

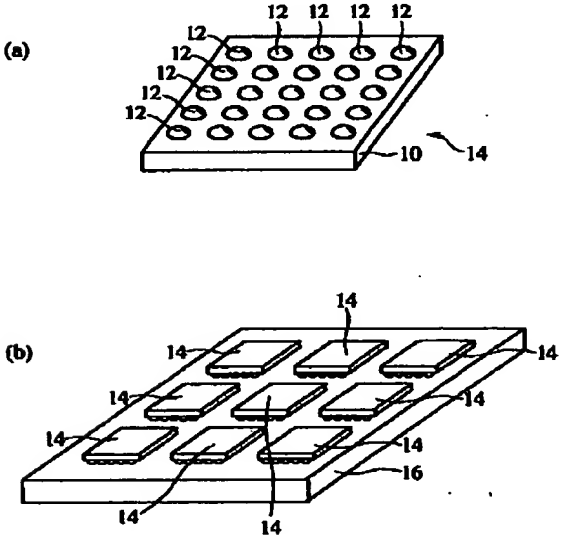
【図６】本発明の第２実施形態において疲労寿命試験を行った手順を示す図である。

【符号の説明】

１０…半導体素子
１２…はんだバンプ
１４…半導体装置
１６…回路基板
１８…基板
２０…キャップ
２２…半導体パッケージ
２４…電極
２６…電極
２８…スタッドバンプ
３０…接合
３２…メタルマスク

【図１】

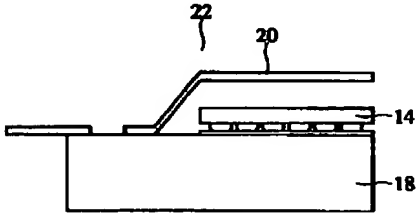
本発明の第1実施形態による半導体装置の構造を示す概略図



10…半導体基板
12…はんだバンプ
14…半導体装置
16…回路基板

【図２】

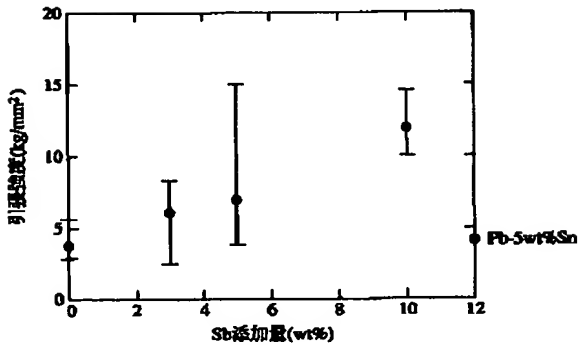
本発明の第1実施形態の変形例による半導体装置の構造を示す概略断面図



14…半導体装置
18…基板
20…キャップ
22…半導体パッケージ

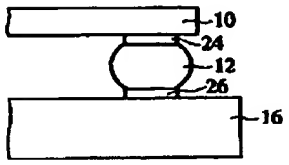
【図３】

Sn-Sb系はんだの引っ張り強度とSb添加量との関係を示すグラフ



【図４】

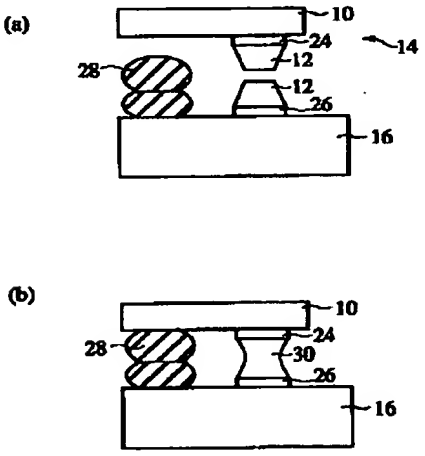
はんだバンプの形状による問題を説明する図



10…半導体基板
12…はんだバンプ
16…回路基板
24…電極
26…電極

【図５】

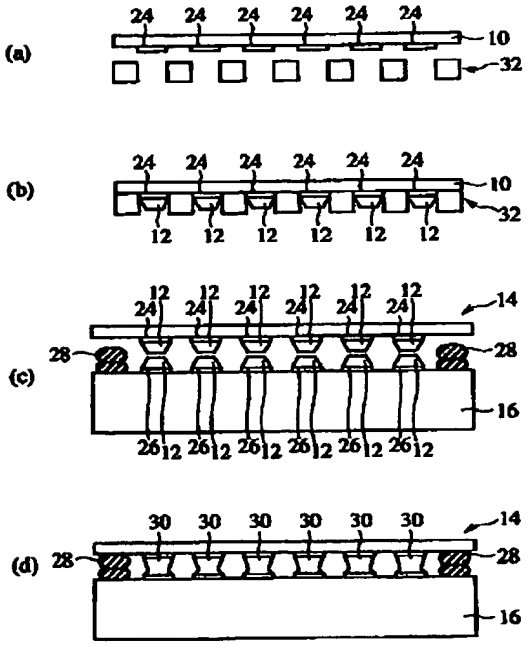
本発明の第2実施形態による半導体装置の構造を示す概略図



10…半導体基板　24…電極
12…はんだバンプ　26…電極
14…半導体装置　28…スタッドバンプ
16…回路基板　30…接合

【図６】

本発明の第2実施形態において疲労寿命試験を行った手順を示す図



10…半導体基板　26…電極
12…はんだバンプ　28…スタッドバンプ
14…半導体装置　30…接合
16…回路基板　32…メタルマスク
24…電極

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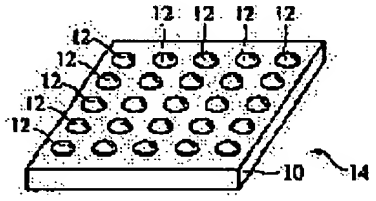
(54) SEMICONDUCTOR DEVICE, CIRCUIT BOARD AND ELECTRONIC CIRCUIT DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To reduce alpha rays emitted from a solder bump and reduce the soft error inversion ratio of a semiconductor device, by causing a solder alloy to be an alloy of Sn and Bi or an element having a specified atomic number and not related with specified alpha decay.

SOLUTION: A solder bump 12 is formed on a pad electrode of a semiconductor substrate 10 by a plating method and a solder ball, thus forming a semiconductor device 14. A solder alloy is caused to be an alloy of Sn and Bi or an element having an atomic number smaller than 81 and not related with alpha decay. Among elements having atomic numbers smaller than the atomic number 82 of Pb, there exists no element related with decay series, such as, U and Th. Therefore, no alpha decay is generated and hence no alpha ray is emitted. Thus, the soft error inversion ratio of the semiconductor device 14 may be reduced. Also, by reducing the quantity of alpha rays emitted from the solder alloy, the solder bump 12 may be arranged in a matrix. Therefore, finer pad diameter and pitch size of the bump are not necessary and deterioration in fatigue life of the solder bump 12 may be prevented.



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CLAIMS

[Claim(s)]

[Claim 1] It is the semiconductor device characterized by Sn, Bi, or the atomic number being an alloy with the element with which the aforementioned solder does not participate in less than 81 alpha decay in the semiconductor device which has the solder bump who consists of a solder which was formed through the insulator layer on the semiconductor substrate in which the semiconductor device was formed, and the aforementioned semiconductor substrate, and was formed on the electrode connected to the aforementioned semiconductor device, and the aforementioned electrode.

[Claim 2] The semiconductor device characterized by the amount of Pb contained in a semiconductor device according to claim 1 in Sn which constitutes the aforementioned solder being 1 ppm or less.

[Claim 3] It is the semiconductor device characterized by the aforementioned solder containing Above Sn as the most components in a semiconductor device according to claim 1 or 2.

[Claim 4] The semiconductor device characterized by having a wrap package for the support substrate by which flip chip junction of the aforementioned semiconductor substrate was done by the aforementioned solder bump, and the aforementioned semiconductor substrate further in a semiconductor device according to claim 1 to 3.

[Claim 5] It is the semiconductor device characterized by the configuration of the aforementioned solder [in / the joint of the aforementioned semiconductor substrate and the aforementioned support substrate / on a semiconductor device according to claim 4 and] being a waist configuration where the center section was narrow.

[Claim 6] The circuit board characterized by having a support substrate, the electrode formed on the aforementioned support substrate, and the solder bump according to claim 1 to 3 formed on the aforementioned electrode.

[Claim 7] Electronic-circuitry equipment characterized by having the semiconductor device according to claim 1 to 3 by which flip chip junction was carried out on the front face of the circuit board and the aforementioned circuit board.

[Claim 8] It is electronic-circuitry equipment characterized by the configuration of the aforementioned solder [in / the joint of the aforementioned semiconductor device and the aforementioned circuit board / on electronic-circuitry equipment according to claim 7 and] being a waist configuration where the center section was narrow.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to the technology which joins a semiconductor device to the circuit board etc. by the flip chip conjugation method, and relates to the semiconductor device, the circuit board, and electronic-circuitry equipment which fitted the flip chip conjugation method especially.
[0002]
[Description of the Prior Art] Conventionally, the terminal pad of LSI was formed in the periphery section of the field which has arranged the element. As the typical junction method which joins an element and a terminal, the wirebonding method was mainly used. However, with high integration of LSI in recent years, the formation of a many-items child of the number of input/output terminals and detailed-ization of the pitch between terminals advance, and the case where it cannot respond is increasing by the pad arrangement to the conventional periphery section.
[0003] Then, since it corresponds to such many-items child-ization, a pad is arranged in the shape of an array on an element field, and the flip chip junction technology of mounting this in the circuit board by the solder bump is developed. In flip chip mounting, since direct LSI and a substrate are joined using a solder bump, there is the feature that a signal can be spread at high speed. Moreover, since a solder bump can form by the vacuum deposition or the galvanizing method, she has the feature of being able to respond to detailed-ization of a terminal easily.
[0004] In addition, as a solder material used for flip chip junction, the alloy of the Pb-Sn system which made Pb (lead) the principal component was mainly used.
[0005]
[Problem(s) to be Solved by the Invention] Five kinds of isotopes, 214Pb, 212Pb, 210Pb, 208Pb, and 206Pb, are included in Pb used as a solder material. Since these isotopes were accompanied by the alpha decay which is an intermediate product in U (uranium) and Th (thorium) radioactive series, or an end product; and emits helium atomic nucleus in the case of decay, alpha rays might produce them from the inside of solder.
[0006] For this reason, in flip chip mounting which stations a solder bump in the shape of an array to the active region of LSI, the soft error might arise by the alpha rays generated from the isotope and alpha decay nature impurity of Pb which are contained in a solder bump. on the other hand, it is put in practical use now -- most -- high -- the soft error is reduced when impurity contents to which the gate length of a transistor participates in the alpha decay produced from the old mine in these elements although the supply voltage between 0.5-0.75 micrometers and a source-drain was about 2.5-3.0V, such as U and Th, constitute solder from a CMOS device [****] using few Pb (the amount of alpha rays is about two about 1 cph/cm)
[0007] However, in order to stop the calorific value which the gate number and the number of terminals are increasing, and is produced from an element with high integration of LSI in recent years, it is necessary to set up supply voltage low. In connection with this, the amount of maximum collection charges in the diffusion layer of N+ or P+ also becomes low. Moreover, in order to raise a degree of integration, also in the gate length of a transistor, detailed-ization is advancing. For this reason, although it becomes indispensable to set supply voltage as less than [2.0V] from now on, and to set gate length as 0.25 micrometers or less from now on, since a semiconductor device becomes sensitive to the turbulence current generated by alpha rays by carrying out like this, there is a possibility of becoming easy to start a soft error.
[0008] supply voltage -- 0.5V -- when it became low, about 2 figures of reversal incidence rates became high, since the amount of collection charges decreased similarly when gate length decreased, the cure against a soft error needed to be strengthened with detailed-izing of an element, and solder material which can reduce the rate of a soft

error was desired The purpose of this invention is to offer the solder material which can reduce a soft error and offer further the semiconductor device and the circuit board which used this for the solder bump, and electronic-circuitry equipment.
[0009]
[Means for Solving the Problem] The aforementioned solder is attained by the semiconductor device characterized by for Sn, Bi, or the atomic number to be an alloy with the element which does not participate in less than 81 alpha decay in the semiconductor device which has the solder bump who consists of a solder which the above-mentioned purpose was formed through the insulator layer on the semiconductor substrate in which the semiconductor device was formed, and the aforementioned semiconductor substrate, and was formed on the electrode connected to the aforementioned semiconductor device, and the aforementioned electrode. Thus, by constituting a semiconductor device, the alpha rays generated from a solder bump can be decreased. Thereby, the rate of soft error reversal of a semiconductor device can be reduced sharply.
[0010] Moreover, since a solder bump can be stationed in the shape of a matrix by reducing the amount of alpha rays generated from a solder, it is not necessary to make detailed a bump's diameter of a pad, and pitch size, and the fall of a solder bump's fatigue life can be prevented. Moreover, when low-battery-ization of the detailed-izing and supply voltage of a semiconductor device progresses further, a soft error can be prevented effectively.
[0011] Moreover, in the above-mentioned semiconductor device, it is desirable for the amount of Pb contained in Sn which constitutes the aforementioned solder to be 1 ppm or less. Thus, by decreasing the content of Pb, the probability which carries out alpha decay can be reduced to or less conventional 1 / ten to 1/100. Therefore, the rate of a soft error can be reduced sharply. Moreover, as for the aforementioned solder, in the above-mentioned semiconductor device, it is desirable to contain Above Sn as the most components.
[0012] Moreover, in the above-mentioned semiconductor device, it is desirable to have a wrap package for the support substrate by which flip chip junction of the aforementioned semiconductor substrate was done by the aforementioned solder bump, and the aforementioned semiconductor substrate further. Thus, if a semiconductor device is constituted, the strong semiconductor package of soft error resistance can be formed. Moreover, as for the configuration of the aforementioned solder in the joint of the aforementioned semiconductor substrate and the aforementioned support substrate, in the above-mentioned semiconductor device, it is desirable that it is the waist configuration where the center section was narrow. Thus, if a semiconductor device is constituted, since the stress concerning an electrode can be distributed, the fall of the fatigue life of solder can be prevented.
[0013] Moreover, it is attained by the circuit board characterized by having a support substrate, the electrode formed on the aforementioned support substrate, and the above-mentioned solder bump formed on the aforementioned electrode. Thus, by constituting the circuit board, soft error generating at the time of carrying a semiconductor device on the circuit board can be reduced. Moreover, it is attained on the front face of the circuit board and the aforementioned circuit board by the electronic-circuitry equipment characterized by having the above-mentioned semiconductor device by which flip chip junction was carried out. Thus, since the malfunction of the semiconductor device by the soft error etc. can be decreased if electronic-circuitry equipment is constituted, the reliability of electronic-circuitry equipment can be raised.
[0014] Moreover, as for the configuration of the aforementioned solder in the joint of the aforementioned semiconductor device and the aforementioned circuit board, in above electronic-circuitry equipment, it is desirable that it is the waist configuration where the center section was narrow. Thus, if a semiconductor device is constituted, since the stress concerning an electrode can be distributed, the fall of the fatigue life of a joint can be prevented. Thereby, the reliability of electronic-circuitry equipment can be improved.
[0015]
[Embodiments of the Invention] The semiconductor device by the 1st operation gestalt of this invention is explained using drawing 1 and drawing 2 . The schematic diagram and drawing 2 which show the structure of the semiconductor device according [drawing 1] to this operation gestalt are the outline cross section showing the structure of the semiconductor device by the modification of this operation gestalt.
[0016] The method of preparing systematic safeguards, such as the method of applying the coating agent which has an alpha-rays shielding effect in a chip front face as a method of conventionally preventing the soft error by alpha rays, the method of changing the layout of the bump on LSI and enlarging distance to the source of alpha rays and an element, and error correction, the method of reducing the impure amount of resources used as the source of alpha rays included in solder material, etc. were used.
[0017] In the conventional CMOS device, the bump has been stationed so that the distance to the source of alpha rays and an active region may separate as much as possible, and soft error reversal has been prevented. However, if a degree of integration will become still higher from now on, it will be necessary to station a solder bump also on

an element. Moreover, if alpha-rays prevention by layout change of a bump is performed, although it is necessary to make detailed further a bump's diameter of a pad, and pitch size, it is necessary to secure the fatigue life by this stress enough repeatedly in this case.

[0018] The method of reducing the source of alpha rays included in solder material to these methods is very effective. However, in the Sn-Pb system solder used conventionally, in the usual chemical treatment, it was impossible to have removed the isotope of Pb which participates in alpha decay, and it was not desirable from the field of material cost.

[0019] Then, the invention-in-this-application person etc. considered constituting solder using the material which does not participate in alpha decay instead of the conventional Pb as a means to reduce a soft error. It was realized that the solder which consists of Bi (bismuth) or Pb by the element with the small atomic number and which used Sn (tin) as the base was specifically used. That is, in an element with the atomic number smaller than 81 of Pb, it is because alpha rays do not arise since alpha decay does not occur, since the element in connection with radioactive series, such as U and Th, does not exist. Moreover, it is because the half-life is as short as 19.9 minutes, and high-grade-izing is easy about Bi since there are also few abundance ratios of the isotope, although an isotope exists in radioactive series, such as U and Th.

[0020] In this case, even if the element in connection with radioactive series contains as an impurity in each element, compared with the isotope removal in Pb, high-grade-izing of material is comparatively easy, and can make material cost cheap. In addition, as an element with the atomic number smaller than 81 of Pb, Sb (antimony), Ag (silver), Zn (zinc), etc. can be used, for example.

[0021] Furthermore, the invention-in-this-application person found out that it was important to reduce Pb content, respectively about the composition element of solder. For example, although the Sn-Sb system solder used conventionally emitted little alpha rays, even if it removed U and Th which participate in alpha decay as much as possible out of Sn-Sb solder, the amount of alpha rays was not fully able to be reduced.

[0022] As a result of an invention-in-this-application person's etc. investigating about this cause, it found out that alpha rays had occurred by the alpha decay of the isotope (214Pb(s) with an especially short half-life, 212Pb, 210Pb) of Pb contained as an impurity in Sn. Then, when the amount of content Pb(s) in Sn was decreased, it turns out that the amount of alpha rays can be reduced. That is, the probability which carries out alpha decay was able to be reduced by holding down Pb concentration to 1 ppm or less to or less conventional 1 / ten to 1/100.

[0023] Next, the semiconductor device using the above-mentioned solder as a solder bump is constituted, and the result which evaluated about soft error resistance is shown. First, the CMOS device constituted by n type MOS transistor and p type MOS transistor was formed according to the manufacture process of the usual MOS transistor on the p type silicon substrate.

[0024] Subsequently, the pad electrode which consists of the wiring layer which consists of aluminum (aluminum) of about 1 micrometer of thickness, Ti (titanium) film of about 100nm of thickness, a nickel (nickel) film of about 200nm of thickness, and an Au(gold) film of about 200nm of thickness was formed through the insulating layer of about 500nm of thickness on the silicon substrate in which the CMOS device was formed. In this way, the semiconductor substrate 10 by which the semiconductor device was formed and the pad electrode was formed in the front face in the shape of a matrix was formed.

[0025] Then, using the various solders shown in Table 1, on the pad electrode of the semiconductor substrate 10, the solder bump 12 was formed and the semiconductor device 14 was formed with the galvanizing method and the solder ball (drawing 1 (a)). In addition, the dross-inclusion concentration of Pb used the thing 1 ppm or less for Sn raw material which constitutes a solder. Then, flux was applied to the front face of the semiconductor device 14 formed in this way, and flip chip junction was carried out on the circuit board 16 which consists of AlN in a conveyer furnace (drawing 1 (b)). At this time, the solder bump's 12 path was 100 micrometers, and the pitch between the solder bumps 12 was 210 micrometers.

[0026] Thus, the rate of soft error reversal was measured about the semiconductor device 14 carried on the circuit board 16. In addition, the rate of soft error reversal generated alpha rays to the semiconductor device 14 using Po (polonium) standard sample (dose : 8.0x10 -3 Bq), and was measured with the circuit tester. Moreover, the amount of alpha rays in solder material was measured by the alpha-truck method.

[0027] Consequently, as shown in Table 1, (the example 1 or the example 16), and the rate of soft error reversal were able to acquire the ten to 2 fit/bit [less than] value by using the solder which consists of Bi or Pb by the element with the small atomic number and which used Sn as the base instead of Pb. That is, as compared with the conventional Pb-5wt%Sn solder shown in the examples 1 and 2 of comparison, the rate of 2 or more figures low soft error reversal was able to be attained.

[0028]

[Table 1]

	はんだ合金 (組成はwt%)	α線量 cph/cm²	純度	Sn中のPb量 ppn	ソフトエラー反転率 fit/bit
実施例1	95Sn-5Zn	<0.1	5N	<1	<0.01
実施例2	90Sn-10Zn	<0.1	5N	<1	<0.01
実施例3	95.5Sn-3.5Ag-1Zn	<0.1	5N	<1	<0.01
実施例4	92Sn-3Ag-5Zn	<0.1	5N	<1	<0.01
実施例5	88Sn-2Ag-10Zn	<0.1	5N	<1	<0.01
実施例6	95Sn-5Sb	<0.1	5N	<1	<0.01
実施例7	90Sn-10Sb	<0.1	5N	<1	<0.01
実施例8	95.5Sn-3.5Ag-1Sb	<0.1	5N	<1	<0.01
実施例9	92Sn-3Ag-5Sb	<0.1	5N	<1	<0.01
実施例10	88Sn-2Ag-10Sb	<0.1	5N	<1	<0.01
実施例11	95Sn-5Bi	<0.1	5N	<1	<0.01
実施例12	90Sn-10Bi	<0.1	5N	<1	<0.01
実施例13	95.5Sn-3.5Ag-1Bi	<0.1	5N	<1	<0.01
実施例14	92Sn-3Ag-5Bi	<0.1	5N	<1	<0.01
実施例15	88Sn-2Ag-10Bi	<0.1	5N	<1	<0.01
実施例16	96.5Sn-3.5Ag	<0.1	5N	<1	<0.01
比較例1	5Sn-95Pb	1.0	4N		0.1
比較例2	5Sn-95Pb	10.0	4N		1

Therefore, if the solder bump for flip chip junction is formed using such a solder, the rate of soft error reversal of a semiconductor device can be reduced sharply. Moreover, since a solder bump can be stationed in the shape of a matrix by reducing the amount of alpha rays generated from a solder, it is not necessary to make detailed a bump's diameter of a pad, and pitch size, and the fall of a solder bump's fatigue life can be prevented.

[0029] Moreover, when low-battery-ization of the detailed-izing and supply voltage of a semiconductor device progresses further, a soft error can be prevented effectively. In addition, although the above-mentioned operation gestalt explained the case where a semiconductor device was joined on the circuit board, you may join a semiconductor device to other substrates. For example, as shown in drawing 2 , a cap 20 may be put on the semiconductor device 14 joined on the substrate 18, and a semiconductor package 22 may be formed. Moreover, on the circuit board, a semiconductor device may be joined and a multi chip module may be formed.

[0030] Moreover, in the above-mentioned operation gestalt, in case a solder is constituted, it is effective to make it the most components in a solder serve as Sn. Next, the semiconductor device by the 2nd operation gestalt of this invention is explained using drawing 3 or drawing 6 . The graph with which drawing 3 shows the relation between the tensile strength of Sn-Sb system solder and Sb addition, drawing where drawing 4 explains the problem by a solder bump's configuration, the schematic diagram showing the structure of the semiconductor device according [drawing 5] to this operation gestalt, and drawing 6 are drawings showing the procedure which performed the fatigue-life examination in this operation gestalt.

[0031] If the solder bump for flip chip junction is formed using Sn system solder in the 1st operation gestalt, the rate of soft error reversal of a semiconductor device can be reduced sharply. However, the degree of hardness compares with Sn-Pb system solder, and the above-mentioned Sn system solder is a stiff. For example, as Sn-Sb system solder shows to drawing 3 , the tensile strength is 2 seven to 15 kgf/mm, and is larger than 3.5kgf/mm2 of Sn-Pb system solder.

[0032] For this reason, if it joins by solder for example, using the solder bump 12 as shows drawing 4 , stress will concentrate on electrodes 24 and 26 in the case of junction, and we will be anxious about bringing about the fall of a fatigue life. This operation gestalt shows the structure of the semiconductor device which stress does not concentrate on an electrode in the case of junction.

[0033] The semiconductor device by this operation gestalt has the feature in constituting so that the configuration of

the solder after junction may turn into the waist configuration where the center section was narrow. That is, on the electrode 24 formed in the semiconductor substrate 10, the solder bump 12 formed so that the upper part might become thin is formed. On the other hand, the solder bump 12 formed so that the upper part might become thin is formed also on the electrode 26 on the circuit board 16 which carries a semiconductor device 14. Moreover, the stud bump 28 for making distance of the semiconductor substrate 10 and the circuit board 16 to join into a predetermined value further is formed in the circuit board 16.

[0034] Thus, if the formed semiconductor device 14 is joined to the circuit board 16, the junction 30 by the solder in which the center section was narrow will be formed of the solder bump 12 of a semiconductor device 14, and the solder bump 12 of the circuit board 16. The interval between a semiconductor device 14 and the circuit board 16 is controlled by the stud bump 28 by desired distance.

[0035] Since the stress concentration given to electrodes 24 and 26 in the case of junction by constituting the semiconductor device 14 and the circuit board 16 which have such a solder bump 12 is mitigable, when flip chip junction is performed using the above-mentioned Sn system solder, the fall of the fatigue life of the soldered joint section can be suppressed. Next, the result which performed fatigue-life evaluation is explained using drawing 6 about the semiconductor device by this operation gestalt.

[0036] First, the semiconductor substrate 10 of 13mm angle which has arranged the electrode 24 in the shape of a matrix was created as a sample for fatigue-life evaluation. The electrode 24 formed Ti film of about 100nm of thickness, nickel film of about 200nm of thickness, and Au film of about 200nm of thickness by the cascade screen deposited one by one by the spatter. Subsequently, the solder bump 12 was formed on the electrode 26 of the circuit board 16, and the electrode 24 of the semiconductor substrate 10, using as a solder the Sn-5wt%Sb alloy which set Pb concentration in solder material to 1 ppm or less. Moreover, the stud bump 28 who consists of Au was formed in the four corners on the circuit board 16. A stud bump's height was adjusted so that the height of the solder bump after junction might be set to 120 micrometers.

[0037] The solder bump formed by carrying out the vacuum evaporationo of the solder 12, after covering the semiconductor substrate 10 with the metal mask 32, as shown in drawing 6 (a). Thus, by forming the solder bump 12, the upper part can form the solder bump 12 of a narrow configuration (drawing 6 (b)). Thus, the solder bump 12 formed the semiconductor device formed on the semiconductor substrate 10.

[0038] Then, after applying flux to a front face, flip chip junction to a semiconductor device 14 and the circuit board 16 was performed by performing alignment of a semiconductor device 14 and the circuit board 16 (drawing 6 (c)), and performing a reflow all over a conveyer furnace (drawing 6 (d)). Thus, the joined junction 30 was a waist configuration 210 micrometers and whose bump height the pitch between about 100 micrometers and a bump is 120 micrometers for the path.

[0039] Then, as a result of performing a -65-125-degree C spalling test for the flip chip zygote formed in this way, the examination of 100 cycle could be cleared and it turns out that it has the fatigue life of the same grade as Pb-5wt%Sn solder. Thus, since according to this operation gestalt it constituted so that the configuration of the solder bump after junction might turn into the waist configuration where the center section was narrow, using Sn system solder in the 1st operation gestalt, it can suppress that stress concentrates on an electrode in the case of junction. Thereby, a fatigue life equivalent to Pb-Sn system solder is securable.

[0040] Moreover, with this operation gestalt, since the solder used for the semiconductor device by the 1st operation gestalt is applied also to the electrode 26 on the circuit board 16, the reliability of the electronic-circuitry equipment with which the semiconductor device was carried in the circuit board can also be raised. In addition, although the above-mentioned operation gestalt explained the case where a semiconductor device was carried in the circuit board, in case the semiconductor package shown in drawing 2 is formed, it can apply. That is, in case a semiconductor device 14 is joined to a substrate 18, it can carry out by the method shown in drawing 6 .

[0041]

[Effect of the Invention] The semiconductor substrate in which, as for the above-mentioned purpose, the semiconductor device was formed according to this invention the above passage, In the semiconductor device which has the solder bump who consists of a solder which was formed through the insulator layer on the semiconductor substrate, and was formed on the electrode connected to the semiconductor device, and the electrode As a solder, since Sn, Bi, or the atomic number uses an alloy with less than 81 element which does not carry out alpha decay, the alpha rays generated from a solder bump can be reduced. Thereby, the rate of soft error reversal of a semiconductor device can be reduced sharply.

[0042] Moreover, since a solder bump can be stationed in the shape of a matrix by reducing the amount of alpha rays generated from a solder, it is not necessary to make detailed a bump's diameter of a pad, and pitch size, and the fall of a solder bump's fatigue life can be prevented. Moreover, when low-battery-ization of the detailed-izing and

supply voltage of a semiconductor device progresses further, a soft error can be prevented effectively.
[0043] Moreover, in the above-mentioned semiconductor device, if the amount of Pb contained in Sn which constitutes a solder is set to 1 ppm or less, the probability which carries out alpha decay can be reduced to or less conventional 1 / ten to 1/100. Thereby, the rate of a soft error can be reduced. Moreover, as for a solder, in the above-mentioned semiconductor device, it is desirable to contain Sn as the most components.
[0044] Moreover, in the above-mentioned semiconductor device, if a wrap package is further prepared for the support substrate by which flip chip junction of the semiconductor substrate was done by the solder bump, and a semiconductor substrate, the strong semiconductor package of soft error resistance can be formed. Moreover, in the above-mentioned semiconductor device, if the configuration of the solder in the joint of a semiconductor substrate and a support substrate is made into the waist configuration where the center section was narrow, since the stress concerning an electrode can be distributed, the fall of the fatigue life of solder can be prevented.
[0045] Moreover, since a support substrate, the electrode formed on the support substrate, and the above-mentioned solder bump formed on the electrode constitute the circuit board, soft error generating at the time of carrying a semiconductor device on this circuit board can be reduced. Moreover, if the above-mentioned semiconductor device by which flip chip junction was carried out constitutes electronic-circuitry equipment on the front face of the circuit board and the circuit board, since the malfunction of the semiconductor device by the soft error etc. can be decreased, the reliability of electronic-circuitry equipment can be raised.
[0046] Moreover, in above electronic-circuitry equipment, if the configuration of the solder in the joint of a semiconductor device and the circuit board is made into the waist configuration where the center section was narrow, since the stress concerning an electrode can be distributed, the fall of the fatigue life of solder can be prevented.

[Translation done.]

* NOTICES *

1. This document has been translated by computer.So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL FIELD

[The technical field to which invention belongs] this invention relates to the technology which joins a semiconductor device to the circuit board etc. by the flip chip conjugation method, and relates to the semiconductor device, the circuit board, and electronic-circuitry equipment which fitted the flip chip conjugation method especially.

[Translation done.]

PRIOR ART

[Description of the Prior Art] Conventionally, the terminal pad of LSI was formed in the periphery section of the field which has arranged the element. As the typical junction method which joins an element and a terminal, the wirebonding method was mainly used. However, with high integration of LSI in recent years, the formation of a many-items child of the number of input/output terminals and detailed-ization of the pitch between terminals advance, and the case where it cannot respond is increasing by the pad arrangement to the conventional periphery section.

[0003] Then, since it corresponds to such many-items child-ization, a pad is arranged in the shape of an array on an element field, and the flip chip junction technology of mounting this in the circuit board by the solder bump is developed. In flip chip mounting, since direct LSI and a substrate are joined using a solder bump, there is the feature that a signal can be spread at high speed. Moreover, since a solder bump can form by the vacuum deposition or the galvanizing method, she has the feature of being able to respond to detailed-ization of a terminal easily.

[0004] In addition, as a solder material used for flip chip junction, the alloy of the Pb-Sn system which made Pb (lead) the principal component was mainly used.

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention] By this invention, Sn, Bi, or the atomic number uses as a solder an alloy with less than 81 element which does not carry out alpha decay in the semiconductor device which has the solder bump who consists of a solder which the above-mentioned purpose was formed through the insulator layer on the semiconductor substrate in which the semiconductor device was formed, and the semiconductor substrate, and was formed on the electrode connected to the semiconductor device, and the electrode as above. Therefore, the alpha rays generated from a solder bump can be reduced. Thereby, the rate of soft error reversal of a semiconductor device can be reduced sharply.

[0042] Moreover, since a solder bump can be stationed in the shape of a matrix by reducing the amount of alpha rays generated from a solder, it is not necessary to make detailed a bump's diameter of a pad, and pitch size, and the fall of a solder bump's fatigue life can be prevented. Moreover, when low-battery-ization of the detailed-izing and supply voltage of a semiconductor device progresses further, a soft error can be prevented effectively.

[0043] Moreover, in the above-mentioned semiconductor device, if the amount of Pb contained in Sn which constitutes a solder is set to 1 ppm or less, the probability which carries out alpha decay can be reduced to or less conventional 1 / ten to 1/100. Thereby, the rate of a soft error can be reduced. Moreover, as for a solder, in the above-mentioned semiconductor device, it is desirable to contain Sn as the most components.

[0044] Moreover, in the above-mentioned semiconductor device, if a wrap package is further prepared for the support substrate by which flip chip junction of the semiconductor substrate was done by the solder bump, and a semiconductor substrate, the strong semiconductor package of soft error resistance can be formed. Moreover, in the above-mentioned semiconductor device, if the configuration of the solder in the joint of a semiconductor substrate and a support substrate is made into the waist configuration where the center section was narrow, since the stress concerning an electrode can be distributed, the fall of the fatigue life of solder can be prevented.

[0045] Moreover, since a support substrate, the electrode formed on the support substrate, and the above-mentioned solder bump formed on the electrode constitute the circuit board, soft error generating at the time of carrying a semiconductor device on this circuit board can be reduced. Moreover, if the above-mentioned semiconductor device by which flip chip junction was carried out constitutes electronic-circuitry equipment on the front face of the circuit board and the circuit board, since the malfunction of the semiconductor device by the soft error etc. can be decreased, the reliability of electronic-circuitry equipment can be raised.

[0046] Moreover, in above electronic-circuitry equipment, if the configuration of the solder in the joint of a semiconductor device and the circuit board is made into the waist configuration where the center section was narrow, since the stress concerning an electrode can be distributed, the fall of the fatigue life of solder can be prevented.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] Five kinds of isotopes, 214Pb, 212Pb, 210Pb, 208Pb, and 206Pb, are included in Pb used as a solder material. Since these isotopes were accompanied by the alpha decay which is an intermediate product in U (uranium) and Th (thorium) radioactive series, or an end product, and emits helium atomic nucleus in the case of decay, alpha rays might produce them from the inside of solder.

[0006] For this reason, in flip chip mounting which stations a solder bump in the shape of an array to the active region of LSI, the soft error might arise by the alpha rays generated from the isotope and alpha decay nature impurity of Pb which are contained in a solder bump. on the other hand, it is put in practical use now -- most -- high -- the soft error is reduced when impurity contents to which the gate length of a transistor participates in the alpha decay produced from the old mine in these elements although the supply voltage between 0.5-0.75 micrometers and a source-drain was about 2.5-3.0V, such as U and Th, constitute solder from a CMOS device [****] using few Pb (the amount of alpha rays is about two about 1 cph/cm)

[0007] However, in order to stop the calorific value which the gate number and the number of terminals are increasing, and is produced from an element with high integration of LSI in recent years, it is necessary to set up supply voltage low. In connection with this, the amount of maximum collection charges in the diffusion layer of N+ or P+ also becomes low. Moreover, in order to raise a degree of integration, also in the gate length of a transistor, detailed-ization is advancing. For this reason, although it becomes indispensable to set supply voltage as less than [2.0V] from now on, and to set gate length as 0.25 micrometers or less from now on, since a semiconductor device becomes sensitive to the turbulence current generated by alpha rays by carrying out like this, there is a possibility of becoming easy to start a soft error.

[0008] supply voltage -- 0.5V -- when it became low, about 2 figures of reversal incidence rates became high, since the amount of collection charges decreased similarly when gate length decreased, the cure against a soft error needed to be strengthened with detailed-izing of an element, and solder material which can reduce the rate of a soft error was desired The purpose of this invention is to offer the solder material which can reduce a soft error and offer further the semiconductor device and the circuit board which used this for the solder bump, and electronic-circuitry equipment.

[Translation done.]

MEANS

[Means for Solving the Problem] The aforementioned solder is attained by the semiconductor device characterized by for Sn, Bi, or the atomic number to be an alloy with the element which does not participate in less than 81 alpha decay in the semiconductor device which has the solder bump who consists of a solder which the above-mentioned purpose was formed through the insulator layer on the semiconductor substrate in which the semiconductor device was formed, and the aforementioned semiconductor substrate, and was formed on the electrode connected to the aforementioned semiconductor device, and the aforementioned electrode. Thus, by constituting a semiconductor device, the alpha rays generated from a solder bump can be decreased. Thereby, the rate of soft error reversal of a semiconductor device can be reduced sharply.

[0010] Moreover, since a solder bump can be stationed in the shape of a matrix by reducing the amount of alpha rays generated from a solder, it is not necessary to make detailed a bump's diameter of a pad, and pitch size, and the fall of a solder bump's fatigue life can be prevented. Moreover, when low-battery-ization of the detailed-izing and supply voltage of a semiconductor device progresses further, a soft error can be prevented effectively.

[0011] Moreover, in the above-mentioned semiconductor device, it is desirable for the amount of Pb contained in Sn which constitutes the aforementioned solder to be 1 ppm or less. Thus, by decreasing the content of Pb, the probability which carries out alpha decay can be reduced to or less conventional 1 / ten to 1/100. Therefore, the rate of a soft error can be reduced sharply. Moreover, as for the aforementioned solder, in the above-mentioned semiconductor device, it is desirable to contain Above Sn as the most components.

[0012] Moreover, in the above-mentioned semiconductor device, it is desirable to have a wrap package for the support substrate by which flip chip junction of the aforementioned semiconductor substrate was done by the aforementioned solder bump, and the aforementioned semiconductor substrate further. Thus, if a semiconductor device is constituted, the strong semiconductor package of soft error resistance can be formed. Moreover, as for the configuration of the aforementioned solder in the joint of the aforementioned semiconductor substrate and the aforementioned support substrate, in the above-mentioned semiconductor device, it is desirable that it is the waist configuration where the center section was narrow. Thus, if a semiconductor device is constituted, since the stress concerning an electrode can be distributed, the fall of the fatigue life of solder can be prevented.

[0013] Moreover, it is attained by the circuit board characterized by having a support substrate, the electrode formed on the aforementioned support substrate, and the above-mentioned solder bump formed on the aforementioned electrode. Thus, by constituting the circuit board, soft error generating at the time of carrying a semiconductor device on the circuit board can be reduced. Moreover, it is attained on the front face of the circuit board and the aforementioned circuit board by the electronic-circuitry equipment characterized by having the above-mentioned semiconductor device by which flip chip junction was carried out. Thus, since the malfunction of the semiconductor device by the soft error etc. can be decreased if electronic-circuitry equipment is constituted, the reliability of electronic-circuitry equipment can be raised.

[0014] Moreover, as for the configuration of the aforementioned solder in the joint of the aforementioned semiconductor device and the aforementioned circuit board, in above electronic-circuitry equipment, it is desirable that it is the waist configuration where the center section was narrow. Thus, if a semiconductor device is constituted, since the stress concerning an electrode can be distributed, the fall of the fatigue life of a joint can be prevented. Thereby, the reliability of electronic-circuitry equipment can be improved.

[0015]

[Embodiments of the Invention] The semiconductor device by the 1st operation gestalt of this invention is explained using drawing 1 and drawing 2 . The schematic diagram and drawing 2 which show the structure of the semiconductor device according [drawing 1] to this operation gestalt are the outline cross section showing the structure of the semiconductor device by the modification of this operation gestalt.

[0016] The method of preparing systematic safeguards, such as the method of applying the coating agent which has an alpha-rays shielding effect in a chip front face as a method of conventionally preventing the soft error by alpha rays, the method of changing the layout of the bump on LSI and enlarging distance to the source of alpha rays and an element, and error correction, the method of reducing the impure amount of resources used as the source of alpha rays included in solder material, etc. were used.
[0017] In the conventional CMOS device, the bump has been stationed so that the distance to the source of alpha rays and an active region may separate as much as possible, and soft error reversal has been prevented. However, if a degree of integration will become still higher from now on, it will be necessary to station a solder bump also on an element. Moreover, if alpha-rays prevention by layout change of a bump is performed, although it is necessary to make detailed further a bump's diameter of a pad, and pitch size, it is necessary to secure the fatigue life by this stress enough repeatedly in this case.
[0018] The method of reducing the source of alpha rays included in solder material to these methods is very effective. However, in the Sn-Pb system solder used conventionally, in the usual chemical treatment, it was impossible to have removed the isotope of Pb which participates in alpha decay, and it was not desirable from the field of material cost.
[0019] Then, the invention-in-this-application person etc. considered constituting solder using the material which does not participate in alpha decay instead of the conventional Pb as a means to reduce a soft error. It was realized that the solder which consists of Bi (bismuth) or Pb by the element with the small atomic number and which used Sn (tin) as the base was specifically used. That is, in an element with the atomic number smaller than 81 of Pb, it is because alpha rays do not arise since alpha decay does not occur, since the element in connection with radioactive series, such as U and Th, does not exist. Moreover, it is because the half-life is as short as 19.9 minutes, and high-grade-izing is easy about Bi since there are also few abundance ratios of the isotope, although an isotope exists in radioactive series, such as U and Th.
[0020] In this case, even if the element in connection with radioactive series contains as an impurity in each element, compared with the isotope removal in Pb, high-grade-izing of material is comparatively easy, and can make material cost cheap. In addition, as an element with the atomic number smaller than 81 of Pb, Sb (antimony), Ag (silver), Zn (zinc), etc. can be used, for example.
[0021] Furthermore, the invention-in-this-application person found out that it was important to reduce Pb content, respectively about the composition element of solder. For example, although the Sn-Sb system solder used conventionally emitted little alpha rays, even if it removed U and Th which participate in alpha decay as much as possible out of Sn-Sb solder, the amount of alpha rays was not fully able to be reduced.
[0022] As a result of an invention-in-this-application person's etc. investigating about this cause, it found out that alpha rays had occurred by the alpha decay of the isotope (214Pb(s) with an especially short half-life, 212Pb, 210Pb) of Pb contained as an impurity in Sn. Then, when the amount of content Pb(s) in Sn was decreased, it turns out that the amount of alpha rays can be reduced. That is, the probability which carries out alpha decay was able to be reduced by holding down Pb concentration to 1 ppm or less to or less conventional 1 / ten to 1/100.
[0023] Next, the semiconductor device using the above-mentioned solder as a solder bump is constituted, and the result which evaluated about soft error resistance is shown. First, the CMOS device constituted by n type MOS transistor and p type MOS transistor was formed according to the manufacture process of the usual MOS transistor on the p type silicon substrate.
[0024] Subsequently, the pad electrode which consists of the wiring layer which consists of aluminum (aluminum) of about 1 micrometer of thickness, Ti (titanium) film of about 100nm of thickness, a nickel (nickel) film of about 200nm of thickness, and an Au(gold) film of about 200nm of thickness was formed through the insulating layer of about 500nm of thickness on the silicon substrate in which the CMOS device was formed. In this way, the semiconductor substrate 10 by which the semiconductor device was formed and the pad electrode was formed in the front face in the shape of a matrix was formed.
[0025] Then, using the various solders shown in Table 1, on the pad electrode of the semiconductor substrate 10, the solder bump 12 was formed and the semiconductor device 14 was formed with the galvanizing method and the solder ball (drawing 1 (a)). In addition, the dross-inclusion concentration of Pb used the thing 1 ppm or less for Sn raw material which constitutes a solder. Then, flux was applied to the front face of the semiconductor device 14 formed in this way, and flip chip junction was carried out on the circuit board 16 which consists of AlN in a conveyer furnace (drawing 1 (b)). At this time, the solder bump's 12 path was 100 micrometers, and the pitch between the solder bumps 12 was 210 micrometers.
[0026] Thus, the rate of soft error reversal was measured about the semiconductor device 14 carried on the circuit board 16. In addition, the rate of soft error reversal generated alpha rays to the semiconductor device 14 using Po

(polonium) standard sample (dose : 8.0x10 -3 Bq), and was measured with the circuit tester. Moreover, the amount of alpha rays in solder material was measured by the alpha-truck method.
[0027] Consequently, as shown in Table 1, (the example 1 or the example 16), and the rate of soft error reversal were able to acquire the ten to 2 fit/bit [less than] value by using the solder which consists of Bi or Pb by the element with the small atomic number and which used Sn as the base instead of Pb. That is, as compared with the conventional Pb-5wt%Sn solder shown in the examples 1 and 2 of comparison, the rate of 2 or more figures low soft error reversal was able to be attained.
[0028]
[Table 1]

	はんだ合金 (組成はwt%)	α線量 cph/cm²	純度	Sn中のPb量 ppb	ソフトエラー反転率 fit/bit
実施例1	95Sn-5Zn	<0.1	5N	<1	<0.01
実施例2	90Sn-10Zn	<0.1	5N	<1	<0.01
実施例3	95.5Sn-3.5Ag-1Zn	<0.1	5N	<1	<0.01
実施例4	92Sn-3Ag-5Zn	<0.1	5N	<1	<0.01
実施例5	88Sn-2Ag-10Zn	<0.1	5N	<1	<0.01
実施例6	95Sn-5Sb	<0.1	5N	<1	<0.01
実施例7	90Sn-10Sb	<0.1	5N	<1	<0.01
実施例8	95.5Sn-3.5Ag-1Sb	<0.1	5N	<1	<0.01
実施例9	92Sn-3Ag-5Sb	<0.1	5N	<1	<0.01
実施例10	88Sn-2Ag-10Sb	<0.1	5N	<1	<0.01
実施例11	95Sn-5Bi	<0.1	5N	<1	<0.01
実施例12	90Sn-10Bi	<0.1	5N	<1	<0.01
実施例13	95.5Sn-3.5Ag-1Bi	<0.1	5N	<1	<0.01
実施例14	92Sn-3Ag-5Bi	<0.1	5N	<1	<0.01
実施例15	88Sn-2Ag-10Bi	<0.1	5N	<1	<0.01
実施例16	96.5Sn-3.5Ag	<0.1	5N	<1	<0.01
比較例1	5Sn-95Pb	1.0	4N		0.1
比較例2	5Sn-95Pb	10.0	4N		1

Therefore, if the solder bump for flip chip junction is formed using such a solder, the rate of soft error reversal of a semiconductor device can be reduced sharply. Moreover, since a solder bump can be stationed in the shape of a matrix by reducing the amount of alpha rays generated from a solder, it is not necessary to make detailed a bump's diameter of a pad, and pitch size, and the fall of a solder bump's fatigue life can be prevented.
[0029] Moreover, when low-battery-ization of the detailed-izing and supply voltage of a semiconductor device progresses further, a soft error can be prevented effectively. In addition, although the above-mentioned operation gestalt explained the case where a semiconductor device was joined on the circuit board, you may join a semiconductor device to other substrates. For example, as shown in drawing 2 , a cap 20 may be put on the semiconductor device 14 joined on the substrate 18, and a semiconductor package 22 may be formed. Moreover, on the circuit board, a semiconductor device may be joined and a multi chip module may be formed.
[0030] Moreover, in the above-mentioned operation gestalt, in case a solder is constituted, it is effective to make it the most components in a solder serve as Sn. Next, the semiconductor device by the 2nd operation gestalt of this invention is explained using drawing 3 or drawing 6 . The graph with which drawing 3 shows the relation between the tensile strength of Sn-Sb system solder and Sb addition, drawing where drawing 4 explains the problem by a solder bump's configuration, the schematic diagram showing the structure of the semiconductor device according [drawing 5] to this operation gestalt, and drawing 6 are drawings showing the procedure which performed the fatigue-life examination in this operation gestalt.
[0031] If the solder bump for flip chip junction is formed using Sn system solder in the 1st operation gestalt, the rate of soft error reversal of a semiconductor device can be reduced sharply. However, the degree of hardness

compares with Sn-Pb system solder, and the above-mentioned Sn system solder is a stiff. For example, as Sn-Sb system solder shows to drawing 3 , the tensile strength is 2 seven to 15 kgf/mm, and is larger than 3.5kgf/mm2 of Sn-Pb system solder.

[0032] For this reason, if it joins by solder for example, using the solder bump 12 as shows drawing 4 , stress will concentrate on electrodes 24 and 26 in the case of junction, and we will be anxious about bringing about the fall of a fatigue life. This operation gestalt shows the structure of the semiconductor device which stress does not concentrate on an electrode in the case of junction.

[0033] The semiconductor device by this operation gestalt has the feature in constituting so that the configuration of the solder after junction may turn into the waist configuration where the center section was narrow. That is, on the electrode 24 formed in the semiconductor substrate 10, the solder bump 12 formed so that the upper part might become thin is formed. On the other hand, the solder bump 12 formed so that the upper part might become thin is formed also on the electrode 26 on the circuit board 16 which carries a semiconductor device 14. Moreover, the stud bump 28 for making distance of the semiconductor substrate 10 and the circuit board 16 to join into a predetermined value further is formed in the circuit board 16.

[0034] Thus, if the formed semiconductor device 14 is joined to the circuit board 16, the junction 30 by the solder in which the center section was narrow will be formed of the solder bump 12 of a semiconductor device 14, and the solder bump 12 of the circuit board 16. The interval between a semiconductor device 14 and the circuit board 16 is controlled by the stud bump 28 by desired distance.

[0035] Since the stress concentration given to electrodes 24 and 26 in the case of junction by constituting the semiconductor device 14 and the circuit board 16 which have such a solder bump 12 is mitigable, when flip chip junction is performed using the above-mentioned Sn system solder, the fall of the fatigue life of the soldered joint section can be suppressed. Next, the result which performed fatigue-life evaluation is explained using drawing 6 about the semiconductor device by this operation gestalt.

[0036] First, the semiconductor substrate 10 of 13mm angle which has arranged the electrode 24 in the shape of a matrix was created as a sample for fatigue-life evaluation. The electrode 24 formed Ti film of about 100nm of thickness, nickel film of about 200nm of thickness, and Au film of about 200nm of thickness by the cascade screen deposited one by one by the spatter. Subsequently, the solder bump 12 was formed on the electrode 26 of the circuit board 16, and the electrode 24 of the semiconductor substrate 10, using as a solder the Sn-5wt%Sb alloy which set Pb concentration in solder material to 1 ppm or less. Moreover, the stud bump 28 who consists of Au was formed in the four corners on the circuit board 16. A stud bump's height was adjusted so that the height of the solder bump after junction might be set to 120 micrometers.

[0037] The solder bump formed by carrying out the vacuum evaporationo of the solder 12, after covering the semiconductor substrate 10 with the metal mask 32, as shown in drawing 6 (a). Thus, by forming the solder bump 12, the upper part can form the solder bump 12 of a narrow configuration (drawing 6 (b)). Thus, the solder bump 12 formed the semiconductor device formed on the semiconductor substrate 10.

[0038] Then, after applying flux to a front face, flip chip junction to a semiconductor device 14 and the circuit board 16 was performed by performing alignment of a semiconductor device 14 and the circuit board 16 (drawing 6 (c)), and performing a reflow all over a conveyer furnace (drawing 6 (d)). Thus, the joined junction 30 was a waist configuration 210 micrometers and whose bump height the pitch between about 100 micrometers and a bump is 120 micrometers for the path.

[0039] Then, as a result of performing a -65-125-degree C spalling test for the flip chip zygote formed in this way, the examination of 100 cycle could be cleared and it turns out that it has the fatigue life of the same grade as Pb-5wt%Sn solder. Thus, since according to this operation gestalt it constituted so that the configuration of the solder bump after junction might turn into the waist configuration where the center section was narrow, using Sn system solder in the 1st operation gestalt, it can suppress that stress concentrates on an electrode in the case of junction. Thereby, a fatigue life equivalent to Pb-Sn system solder is securable.

[0040] Moreover, with this operation gestalt, since the solder used for the semiconductor device by the 1st operation gestalt is applied also to the electrode 26 on the circuit board 16, the reliability of the electronic-circuitry equipment with which the semiconductor device was carried in the circuit board can also be raised. In addition, although the above-mentioned operation gestalt explained the case where a semiconductor device was carried in the circuit board, in case the semiconductor package shown in drawing 2 is formed, it can apply. That is, in case a semiconductor device 14 is joined to a substrate 18, it can carry out by the method shown in drawing 6 .

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the schematic diagram showing the structure of the semiconductor device by the 1st operation gestalt of this invention.
[Drawing 2] It is the outline cross section showing the structure of the semiconductor device by the modification of the 1st operation gestalt of this invention.
[Drawing 3] It is the graph which shows the relation between the tensile strength of Sn-Sb system solder, and Sb addition.
[Drawing 4] It is drawing explaining the problem by a solder bump's configuration.
[Drawing 5] It is the schematic diagram showing the structure of the semiconductor device by the 2nd operation gestalt of this invention.
[Drawing 6] It is drawing showing the procedure which performed the fatigue-life examination in the 2nd operation gestalt of this invention.
[Description of Notations]
10 -- Semiconductor device
12 -- Solder bump
14 -- Semiconductor device
16 -- Circuit board
18 -- Substrate
20 -- Cap
22 -- Semiconductor package
24 -- Electrode
26 -- Electrode
28 -- Stud bump
30 -- Junction
32 -- Metal mask

[Translation done.]

* NOTICES *

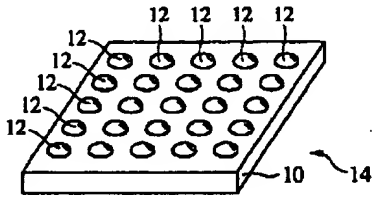
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

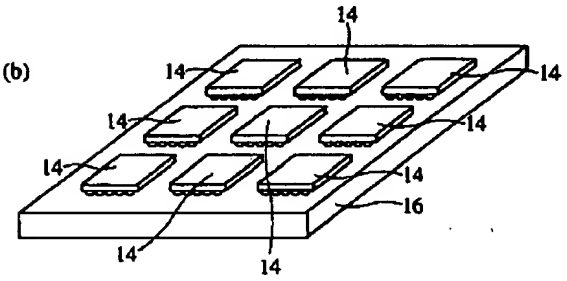
[Drawing 1]

本発明の第1実施形態による半導体装置の
構造を示す概略図

(a)



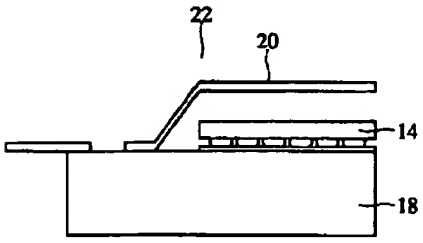
(b)



10…半導体基板
12…はんだバンプ
14…半導体装置
16…回路基板

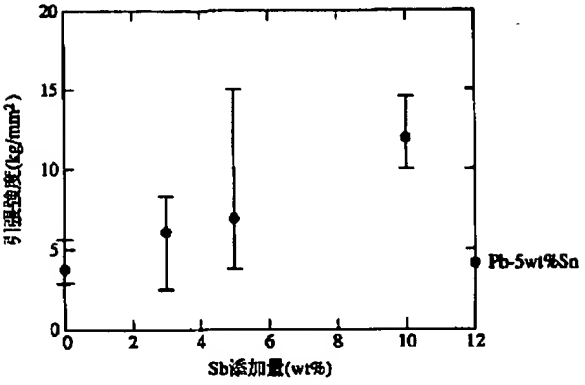
[Drawing 2]

本発明の第1実施形態の変形例による
半導体装置の構造を示す概略断面図

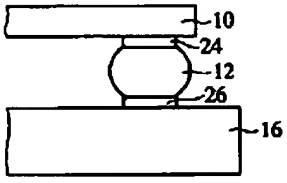


14…半導体装置
18…基板
20…キャップ
22…半導体パッケージ

[Drawing 3]
Sn-Sb系はんだの引っ張り強度とSb添加量
との関係を示すグラフ

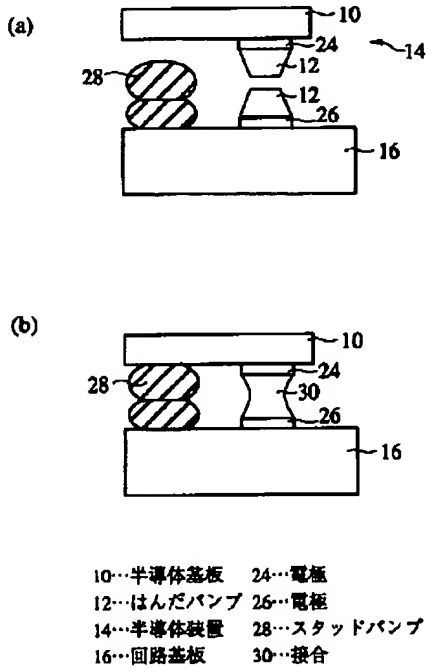


[Drawing 4]
はんだバンプの形状による問題を説明する図



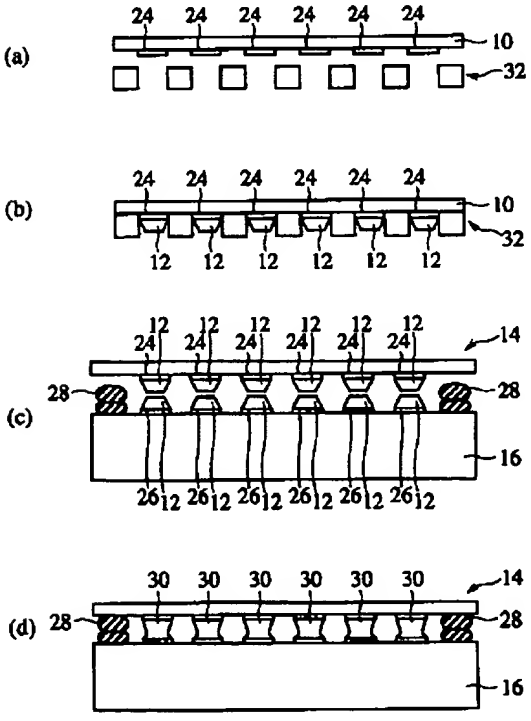
10…半導体基板
12…はんだバンプ
16…回路基板
24…電極
26…電極

[Drawing 5]
本発明の第2実施形態による半導体装置の構造を示す概略図



10…半導体基板　24…電極
12…はんだバンプ　26…電極
14…半導体装置　28…スタッドバンプ
16…回路基板　30…接合

[Drawing 6]
本発明の第2実施形態において疲労寿命試験を行った手順を示す図



10…半導体基板　26…電極
12…はんだバンプ　28…スタッドバンプ
14…半導体装置　30…接合
16…回路基板　32…メタルマスク
24…電極

[Translation done.]